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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,560	02/10/2004	James W. Leith	INSL.0090	1449

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EXAMINER	
ENGLUND, TERRY LEE	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/775,560	LEITH ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Feb 10, 2004 & May 12, 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1 and 2* is/are allowed.

6)☒ Claim(s) *3-10* is/are rejected.

7)☒ Claim(s) *11-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05122005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: Page 13, line 1 "121" should be --111--. On the last line of page 19, "129" should be --229--. Appropriate corrections ere required.

Claim Objections

Claims 3-10, and 14-22 are objected to because of the following informalities: To minimize the possibility that the input of claim 3's amplifier receives both the second reference signal and an output (of some unknown element), it is suggested a comma be added after "input" on line 3 of claim 3, and also after "signal" on line 4 of the same claim. To minimize confusion in claim 14, it is suggested a comma be added after "capacitor" on line 3, and after "amplifier" on line 4. This will more clearly indicate the capacitor develops the startup reference signal, and not the amplifier's second input. Also, --error-- should be added prior to "amplifier" on line 4 of claim 14 for consistent labeling, and to minimize possible confusion with respect to "an amplifier" cited later on claim 14's line 6. Claim 18, line 3 "a third reset state" can be misleading (e.g. the phrase can imply first and second reset states). Therefore, it is suggested the term "reset" be deleted from line 3 of claim 18. Since claim 20, line 3 cites "output switching", it is suggested --the-- be added prior to "output switching" on line 10 of the same claim. For similar reasons, it is suggested "a reference input" on line 2 of claim 21 be changed to --the reference input--. [Note that the phrase's associated "error amplifier" (line 2) and "ramping up" (line 1) are preceded by "the" and "said", respectively within claim 21.] Dependent claims carry over

any objection(s) from any claim(s) upon which they depend. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 11-19, and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. Since the gate control logic and startup circuit can each disable "output switching" (e.g. see lines 6-13) in claim 11, it is not clear how the disabling actually relate to each other. For example, is it the same output switching that is being referred to, and if so, do the logic and circuit disable the switching in their own distinct manner? It is not understood how "operative states" in claim 15 (line 6) relates to the first/second states recited within claim 14. For example, "operative states" can include active, standby (or sleep/idle), power down, high voltage, low voltage, etc. However, since associated claim 18 presently cites "a third reset state", it is suggested line 6 of claim 15 be modified by changing "states" to --states, including the first and second states,-- to more clearly relate the claim's "operative states" to at least the state(s) recited within claims 14 and 18. Claim 22 presently depends on a claim that does not exist. Therefore, it is suggested "210" be changed to --21--. Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

In so far as being understood, claim 11 is rejected under 35 U.S.C. 102(e) as being anticipated by Grant et al. (Grant), a reference cited on the applicants' IDS. Fig. 3 shows a controller for a power converter, wherein the controller comprises error amplifier 20 having first input 22 receiving output sense signal 18, second input 24 receiving startup reference signal 30, and output 32 for providing a compensation signal; gate control logic 40 controls output switching (e.g. of 60 and 62), and disables output switching based on output enable signal SHUTDOWN (e.g. see column 6, lines 21-24); and start up circuit 300,26 is coupled to error amplifier 20. Since 26 generates a sawtooth type signal, it would be understood the startup circuit charges startup reference signal 30 (e.g. during the low to high ramping portion of the signal). Also, since section 300 receives the compensation signal, and provides output enable signal SHUTDOWN, it is understood the startup circuit disables the output switching until the compensation signal achieves some type of an operative level, thus anticipating claim 11.

Claim 20 is rejected under 35 U.S.C. 102(e) as being anticipated by Grant et al. (Grant). The circuit shown in Grant's Fig. 3 can be interpreted as providing a method of startup protection for a DC-DC converter, wherein the method comprises disabling output switching by signal SHUTDOWN; oscillator 26 ramps up voltage 30 at reference input 24 of error amplifier 20, wherein the ramping is based on a reference signal (e.g. CLOCK); error amplifier 20 provides compensation signal 32 based on reference input 24 and a feedback portion (through

86,12) of the DC-DC converter; and since section 300 receives compensation signal 32, it would be understood that its SHUTDOWN signal would be associated with when compensation signal 32 reaches some type of a predetermined regulation level, thus anticipating claim 20.

Claims 20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Umemoto. Fig. 1 shows a circuit that can be considered a method for startup protection of DC-DC converter 1. When transistor Q receives a high signal at its gate, the output switching of the DC-DC converter 1 is disabled; circuit 130a provides ramping up of voltage T that is applied to reference input 131 of error amplifier 13a, and based on a reference signal (e.g. Vs); error amplifier 13a provides a compensation signal (to driver 14) based on reference input 131 and a feedback portion (e.g. see Ve and 11) of output Vo of the DC-DC converter; and when transistor Q is turned on when the compensation signal reaches a predetermined regulation level (i.e. allowing the signal to the gate of transistor Q to reach as least the switching threshold of the transistor), the output switching of DC-DC converter 1 is enabled. Therefore, claim 20 is anticipated. Since ramping up voltage T of reference input 131 is provided by effectively charging capacitor Ca by operational transconductance amplifier 2-4, claim 21 is also anticipated.

Claim 20 is rejected under 35 U.S.C. 102(b) as being anticipated by Yamamaura et al. (Yamamaura), which is reference EP 0 532 263 A1 cited on the IDS submitted by the applicants. Fig. 2 shows a circuit one of ordinary skill in the art would understand provides a method for what can be considered startup protection for DC-DC converter 1, wherein the method comprises disabling output switching by turning transistor 34 off with a logic low signal; section 16 ramps up voltage ST of reference input + of error amplifier 66 based on a reference signal (e.g. from 12 and/or 14); error amplifier 66 provides compensation signal P2 based on the reference input and

a feedback portion (through 61,64) of output Vo; and when compensation signal P2 reaches a predetermined regulation level that allows transistor 34 to conduct, the output switching is effectively enabled, thus claim 20 is anticipated

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 14, 19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grant as applied to their respective claim 11 and 20 described above, and further in view of Dunn et al. (Dunn). As previously described, the reference of Grant shows/discloses a controller comprising an error amplifier, gate control logic, and startup circuit. Although the reference discloses periodic signal source 26 is preferably an oscillator that generates a periodic, sawtooth signal (e.g. see column 3, lines 19-33), the reference does not clearly show/disclose oscillator 26 as a circuit comprising a capacitor and an amplifier. Fig. 1 of Dunn shows one example of a

circuit for generating a sawtooth signal. Therefore, it would have been obvious to one of ordinary skill in the art to replace the (generic) oscillator 26 of Grant with the oscillator type circuit of Dunn. Dunn's circuit comprises a (operational) transconductance amplifier 20 (e.g. see the last three lines of the abstract) with one input receiving voltage reference signal VREF2, and an output coupled to capacitor 32, wherein sawtooth signal VRAMP is developed by the relationships of amplifier 20 and capacitor 32, and is provided as the output. Since this output would correspond to the startup reference signal to second input 24 of Grant's error amplifier 20, and one of ordinary skill in the art would understand the operation of the amplifier would have two states, claims 14 and 19 are rendered obvious. For example, in the first state, amplifier 20 allows current source 34 to charge capacitor 32, and in the second state, amplifier 20 allows current from current source 34 to be diverted away from charging capacitor 32, thus helping to regulate startup reference signal VRAMP (of Dunn)/30 (of Grant). Dunn's circuit will help ensure the amplitude variation of the output signal VRAMP will be substantially consistent, thus providing more accurate operation of the overall circuit (e.g. the charging times will be more consistent). With Dunn's circuit used for Grant's oscillator 26, the ramping up voltage would effectively comprise charging capacitor 32 by (operational) transconductance amplifier 20, rendering claim 21 obvious.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamaura et al. (i.e. reference EP 0 532 263 A1 on the applicants' IDS) as applied to claim 20 described above, and further in view of Dunn et al. (Dunn). As previously described, the reference of Yamamaura shows/discloses a circuit that one of ordinary skill in the art would understand comprises the disabling output switching, ramping up a voltage, providing a compensation signal, and enabling

output switching as recited within claim 20. Although the reference discloses sawtooth circuit for generating a periodic, sawtooth signal (e.g. see Fig. 3), the reference does not clearly show/disclose circuit 10 comprising a capacitor and an amplifier. Fig. 1 of Dunn shows one example of a circuit for generating a sawtooth signal. Therefore, it would have been obvious to one of ordinary skill in the art to replace sawtooth circuit 10 of Yamamaura with the sawtooth type circuit shown in Dunn. This circuit comprises a (operational) transconductance amplifier 20 (e.g. see the last three lines of the abstract) with one input receiving voltage reference signal VREF2, and an output coupled to capacitor 32, wherein the sawtooth signal VRAMP is developed by the relationships of amplifier 20 and capacitor 32, and is provided as the output. With Dunn's circuit used for Yamamaura's circuit 10, ramping up voltage ST would effectively comprise charging capacitor 32 by (operational) transconductance amplifier 20, rendering claim 21 obvious. Dunn's circuit would provide more consistent ramping for more accurate operation of the circuit.

Allowable Subject Matter

Claims 1-2 are allowed. There is presently no motivation to modify or combine any prior art reference(s) to ensure the error amplifier, amplifier circuit, comparator, and startup logic relate to the numerous signals cited (i.e. output sense signal, startup reference signal, compensation signal, second reference signal, start signal, startup complete signal, and output enable signal) as recited within claim 1, upon which claim 2 depends.

Claims 3-10 are only objected to. Claims 4-10 all depend on claim 3, which in turn depends on allowed claim 1. However, the previously described objection of claim 3 should be

addressed/corrected to minimize any possible confusion with respect to what the amplifier's input receives.

Claims 12-13, 15-18, and 22 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. [Note, some of these rejections are carried over from at least one claim upon which they depend.] There is presently no strong motivation to modify or combine any prior art reference(s) to ensure: 1) the comparator compares the compensation signal and predetermined ramp level, and then provides a startup complete signal, as recited within claim 12, upon which claim 13 depends; 2) the startup circuit further comprises a digital state machine for controlling the plurality of switches, and the amplifier's operation states as recited within claim 15, upon which claims 16-19 depend; and 3) the OTA operates in open and closed loop states are recited within claim 22.

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. Although Fig. 1 of Kitagawa could have been used to anticipate claim 20, and modified to render claim 21 obvious, this reference was not cited in any formal rejection described above. However, when transistor 3 opens, the output switching of the DC-DC converter is disabled; it is understood that sawtooth wave generator 12 provides a ramped up voltage to error amplifier 11, which in turn provides a compensation signal based on reference input "-" and a feedback portion (through RIN,10,RC,CC); and once the compensation signal reaches a predetermined regulation level that causes the output of 13 to turn transistor 3 on, the output switching is enabled. Also, it would have been obvious to one of ordinary skill in

the art to replace Kitagawa's (generic) sawtooth wave generator 12 with a circuit comprising an amplifier that charges a capacitor. Lipcsei's figures show a DC-DC converter with a startup circuit. However, since its output switching is related to pullup/pulldown transistors that operate with alternate control, the output switching is never completely disabled, or enabled, (e.g. although one transistor will be disabled, the other transistor will be enabled at any one time). However, these references should still be reviewed and considered with respect to the basic limitations recited within at least the broadest claims.

The prior art references cited on the IDS submitted May 10, 2005 have been reviewed and considered. The Grant et al. reference was used in some of the formal rejections described above. The Savo et al. and Ribellino et al. references both show DC-DC converter type circuits with soft start functions (e.g. startup circuits). Since both of these references show only a single switching device (e.g. see transistor 1 of Savo's Fig. 1; and switch 6 of Ribellino's Fig. 1), it can be considered disabled when it is not conducting, and enabled when it is conducting, and therefore could have been used in the rejections of claims 20 and 21 for the same reasons as described above with respect to the other prior art references cited within the formal rejections. The EP 0 532 263 A reference was used in some of the formal rejections of claims 20 and 21. All four of the above references were identified in the PCT search report also cited on the IDS.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

Kenneth B. Wells
Primary Examiner